I. MARK-UP VERSION AMENDED TO CLAIMS

A. Please amend each of the following claims for the corresponding pending claim in this application:

1. A nonvolatile memory device, comprising:

a substrate of a semiconductor material having a first conductivity type;

a semiconductor block over said substrate and having a first sidewall and a second sidewall opposite to each other and a top between said first sidewall and said second sidewall, said semiconductor block including a first region having a second conductivity type, a second region having said second conductivity type, and a third region between said first region and said second region and having said first conductivity type;

an electrically conductive folded floating gate over said third region of said semiconductor block, said folded floating gate having a first section adjacent said first sidewall of said semiconductor block, a second section adjacent said second sidewall of said semiconductor block, and a third section adjacent said top of said semiconductor block; and

a control gate disposed over said third section of said folded floating gate.

9. The nonvolatile memory device of claim 8, further comprising a second electrically conductive folded floating gate over said sixth region of said semiconductor block, said second folded floating gate having a first section adjacent said first sidewall of said semiconductor block, a second section adjacent said second sidewall of said semiconductor block, and a third section adjacent said top of said semiconductor block.

12. The nonvolatile memory device of claim 10, further comprising:

a second semiconductor block over said substrate and having a first sidewall and a second sidewall opposite to each other and a top between said first sidewall and said second sidewall, said second semiconductor block including:

a first region having said second conductivity type, a second region having said second conductivity type, and a third region between said first

region and said second region and having said first conductivity type; and

a fourth region having said second conductivity type adjacent said second region, a fifth region of said second conductivity type, and a sixth region of said first conductivity type between said fourth region and said fifth region;

a third electrically conductive folded floating gate over said third region of said second semiconductor block, said third folded floating gate having a first section adjacent said first sidewall of said second semiconductor block, a second section adjacent said second sidewall of said second semiconductor block, and a third section adjacent said top of said second semiconductor block;

a fourth electrically conductive folded floating gate over said sixth region of said second semiconductor block, said third folded floating gate having a first section adjacent said first sidewall of said second semiconductor block, a second section adjacent said second sidewall of said second semiconductor block, and a third section adjacent said top of said second semiconductor block; and

a second control gate disposed over said third section of said third folded floating gate and said third section of said fourth folded floating gate.

15. The nonvolatile memory device of claim 1, further comprising:

a second semiconductor block over said substrate and having a first sidewall and a second sidewall opposite to each other and a top between said first sidewall and said second sidewall, said second semiconductor block including a first region having said second conductivity type, a second region having said second conductivity type, and a third region between said first region and said second region and having said first conductivity type;

a second electrically conductive folded floating gate over said third region of said second semiconductor block, said second folded floating gate having a first section adjacent said first sidewall of said second semiconductor block, a second section adjacent said second sidewall of said second semiconductor block, and a third section adjacent said top of said second semiconductor block.

21. A nonvolatile memory device, comprising:

a semiconductor substrate of a first conductivity type;

a plurality of semiconductor blocks over said substrate, each having a first sidewall and a second sidewall, and a top between said first sidewall and said second sidewall, each of said plurality of semiconductor blocks further including a first region of a second conductivity type, a second region of said second conductivity type, and a third region between said first region and said second region and of said first conductivity type;

a plurality of electrically conductive folded floating gates, each over said third region of a corresponding one of said plurality of semiconductor blocks and having a first section, a second section, and a third section adjacent said first sidewall, said second sidewall, and said top, respectively, of said corresponding semiconductor block; and

a plurality of control gates disposed over said plurality of folded floating gates.

27. The nonvolatile memory device of claim 26, further comprising a second plurality of electrically conductive folded floating gates, each over said sixth region of said corresponding semiconductor block and having a first section, a second section, and a third section adjacent said first sidewall, said second sidewall, and said top respectively, of said corresponding semiconductor block.

30. The nonvolatile memory device of claim 21, further comprising:

a second plurality of semiconductor blocks over said substrate, each including a first region of said second conductivity type, a second region of said second conductivity type, and a third region between said first region and said second region and of said first conductivity type;

a second plurality of electrically conductive folded floating gates, each over said third region of a corresponding one of said second plurality of semiconductor blocks; and

wherein said plurality of control gates are further disposed over said second plurality of folded floating gates.

31. A nonvolatile memory array, comprising:

a semiconductor substrate;

a plurality of semiconductor stripes over said substrate substantially parallel to one another, each having a first sidewall and a second sidewall, and a top between said first sidewall and said second sidewall, each of said plurality of stripes further including a plurality of sequentially arranged cells, each cell including a source region, a drain region, and a channel region there between;

a plurality of electrically conductive folded floating gates arranged in a plurality of rows and a plurality of columns, each over said channel region in a corresponding cell and having a first section, a second section, and a third section adjacent said first sidewall, said second sidewall, and said top, respectively, of a corresponding stripe; and

a plurality of control gates, each disposed over a row of said plurality of folded floating gates.